

400Gb/s QSFP112 SR4 100m Transceiver SLT0QPS4400GT85C

Features

- 4x100G PAM4 retimed 400GAUI-4 electrical interface
- MPO-12 APC connector
- 4 channel VCSEL arrays and 4 channels PIN photo detector arrays
- Maximum link length of 60m on OM3 or 100m on OM4
- Hot Pluggable QSFP112 form factor
- Compliant to QSFP112_MSA_Specification_Rev2.1.1
- Compliant with CMIS 5.2
- Compliant with IEEE 802.3db
- Compliant to IEEE 802.3ck
- Power consumption is less than 8W
- Operating case temp
Commercial: 0°C to +70 °C
- RoHS compliant



Applications

- 400GBASE-SR4 400G Ethernet
- Data center

Order Information

Part No.	Bit Rate (Gbps)	Laser (nm)	Distance ¹	Fiber Type	DDMI	Connector	Temp ²
SLT0OPS4400GT85C	425	850	100m	MMF	YES	MPO 1x12	0°C~+70°C

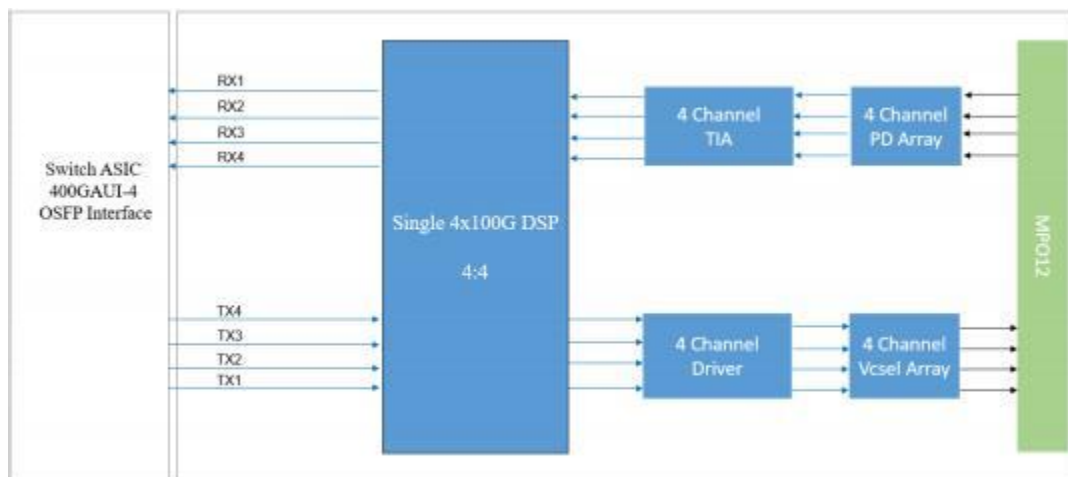
Note:

1. OM4 fiber, 60m for OM3 fiber
2. Case Temperature

I. General Description

SLT0QPS4400GT85C is a four-Channel, Parallel, Pluggable, Fiber-Optic OSFP for 400Gigabit Ethernet applications. This transceiver is a high-performance module for short-range data communication and interconnect application. It integrates four data lanes in each direction with 4x53.125GBd. The length of QSFP112 SR4 is up to 60 meters over OM3 MMF or 100 meters over OM4 MMF. This module is designed to operate over multimode fiber systems using a nominal wavelength of 850nm.

II. Functional Block Diagram



III. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Supply Voltage	Vcc	-0.5	-	+3.6	V	
Storage Temperature	T	-40	-	+85	°C	
Operating Humidity	RH	+15	-	+85	%	1
Receiver Damage Threshold per Lane	P _{IND}	+5	-	-	dBm	

Note: 1 No condensation

IV. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T _C	0	-	+70	°C	
Power Supply Voltage	Vcc	3.14	3.3	3.47	V	
Power Dissipation	P _d	-	-	8	W	
Supply Current				2.55	A	
Bit Rate	BR			425	Gbps	
I2C Clock Frequency		0		400	kHz	

V. Electrical Characteristics

Parameters	Min	Typical	Max	Unit
Pre FEC Bit Error Ratio			2.4E-4	
Post FEC Bit Error Ratio			1E-12	
Transmitter (each Lane)				
Differential pk-pk Input Voltage tolerance	750			mV
Differential Termination Mismatch			10	%
Eye hfour	10			mV
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G-1)			dB
Vertical eye closure			12	dB
Effective return loss	7.3			dB
Transition Time	10			ps
Receiver (each Lane)				
Differential data output swing	300		900	mVpp
Differential termination mismatch			10	%
Eye hfour	15			mV
Vertical eye closure			12	dB
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G-1)			
Effective return loss	8.5			dB
Transition time	8.5			ps

VI. Optical Characteristics

Transmitter Optical Interface					
Parameter	Symbol	Min	Typical	Max	Unit
Data rate per lane	DR		53.125		GBd
Modulation format		PAM4			
Center Wavelength 1	λ	840	860	868	nm
RMS spectral width	σ			0.6	nm
Average Launch power, each lane	Pavg	-1		4	dBm
Optical Power OMA, each Lane , max		3.5			dBm
OMA _{outer} , each lane min	POMA	max (TECQ, TDECQ) < 1.8 dB			max [-2.6 , max(TECQ,TECQ) - 4.4]
		1.8 < max (TECQ, TDECQ) < 4.4 dB			

Transmitter and dispersion eye closure (TDECQ), each lane	TDECQ			4.4	dB
Transmitter eye closure for PAM4 (TECQ), each lane	TECQ			4.4	dB
Extinction ratio	ER	2.5			dB
Transmitter power excursion, each lane				2.3	dBm
Optical Return Loss Tolerance	ORLT			14	dB
Optical Power for TX DISABLE				-30	dBm
Encircled flux _{b2}		≥86% at 19 um ≤30% at 4.5 um			

Note:

1. Defined according to the performance of the laser used.
2. Measured into type A1a.2 or type A1a.3, or A1a.4, 50 um fiber, in accordance with IEC 61280-1-4

Receiver Optical Interface					
Parameter	Symbol	Min	Typical	Max	Unit
Data rate per lane	BR		53.125		Gbd
Modulation format		PAM4			
Center Wavelength	λ	842	850	948	nm
Damage threshold		5			dBm
Average receive power, each lane		-6.4		4	dBm
Receive power, each lane (OMA _{outer})				3.5	dBm
Receiver reflectance	R _r			-15	dB
Receiver sensitivity(OMA), each lane ¹		RS = max (-4.6 , TECQ - 6.4)			dBm
Stressed receiver sensitivity, each lane				-2	dBm
Rx LOS	Assert		-15		dBm
	De-assert			-7.5	dBm
	Hysteresis		0.5	5	dB

Notes:

1. Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

VII. Management Interface

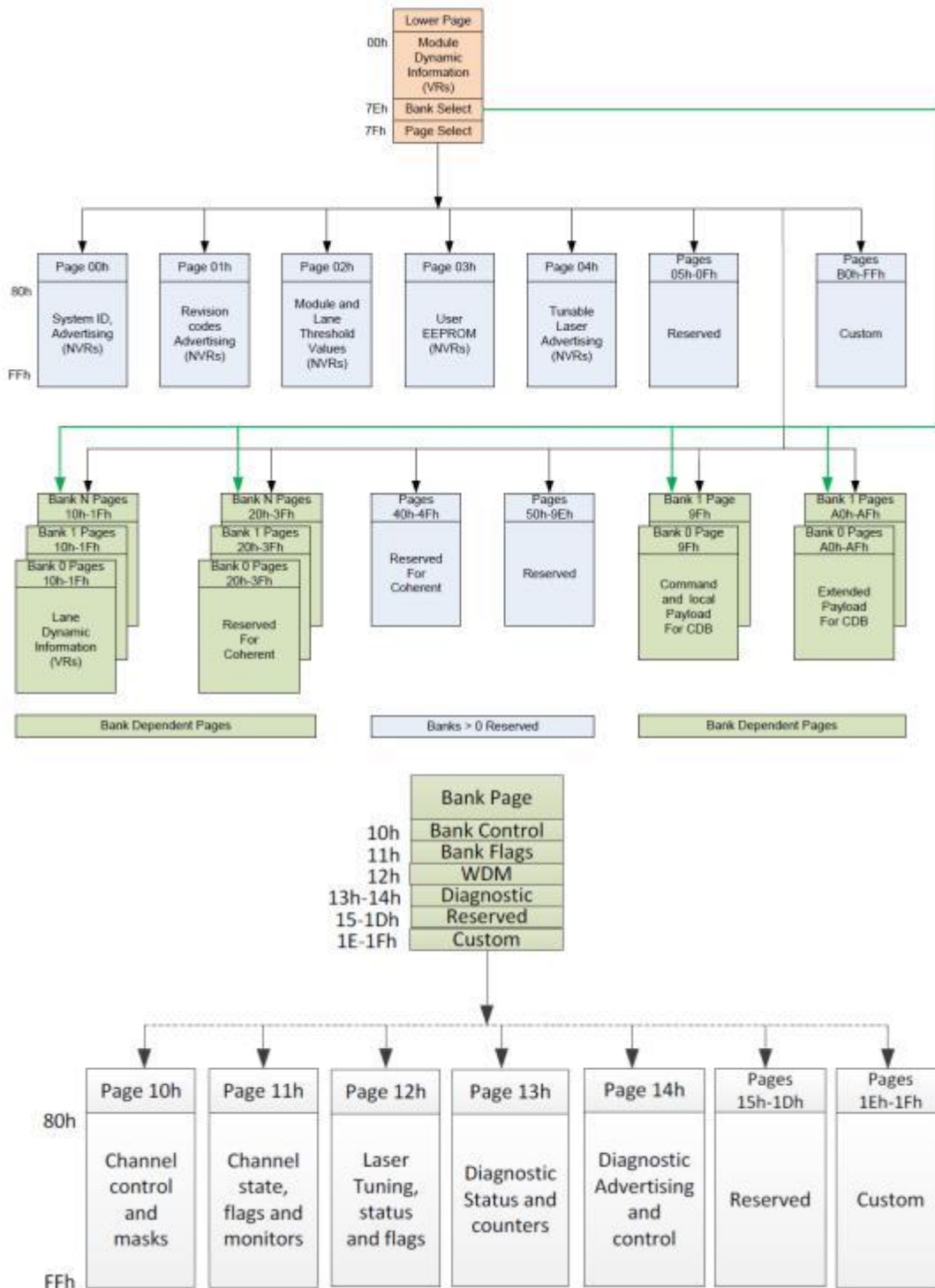


Figure 1, CMIS Module Memory Map

VIII. Multiple Applications Support

The SLT0OPS4400GT85C supports CMIS 5.2 defined Application Advertising, Application Selection and Instantiation.

Application Advertising

Address (Dec)	Application		Value (Hex)	Description
	AppSel Code	Name		
85	NA	Module Type encoding	1	Optical Interfaces: MMF
86	0001b	HostInterfaceID	4B	HostInterfaceIDApp1:100GAUI-1-S C2M
87		MediaInterfaceID	D	MediaInterfaceIDApp1:100GBASE-SR
88		HostLaneCount&MediaLaneCount	11	LaneCountApp1: TX & RX 1 lanes
89		HostLaneAssignmentOptions	F	Permissible first host lane number: lanes 1, 2, 3, 4,
01h:176		MediaLaneAssignmentOptions	F	Permissible first media lane number: lanes 1, 2, 3, 4
90	0010b	HostInterfaceID	F	HostInterfaceIDApp2:200GAUI-4
91		MediaInterfaceID	E	MediaInterfaceIDApp2:200GBASE-SR4
92		HostLaneCount&MediaLaneCount	44	LaneCountApp2:TX & RX 4 lanes
93		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:177		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
94	0011b	HostInterfaceID	C	HostInterfaceIDApp3:100GAUI-4 C2M
95		MediaInterfaceID	0	MediaInterfaceIDApp3: SFF-8024 Undefined
96		HostLaneCount&MediaLaneCount	44	LaneCountApp3:TX & RX 4 lanes
97		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:178		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
98	0100b	HostInterfaceID	4F	HostInterfaceIDApp4:400G S C2M
99		MediaInterfaceID	11	MediaInterfaceIDApp4:400G-SR4
100		HostLaneCount&MediaLaneCount	44	LaneCountApp4:TX & RX 4 lanes
101		HostLaneAssignmentOptions	1	HostLaneAssignmentOptionsApp4:begin lane 1
01h:179		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
102	0101b	HostInterfaceID	4D	HostInterfaceIDApp5:200GAUI-2-S C2M
103		MediaInterfaceID	1B	MediaInterfaceIDApp5:200GBASE-SR2
104		HostLaneCount&MediaLaneCount	22	LaneCountApp5: TX & RX 2 lanes
105		HostLaneAssignmentOptions	5	Permissible first host lane number: lanes 1, 3,
01h:180		MediaLaneAssignmentOptions	5	Permissible first media lane number: lanes 1, 3
106			FF	HostInterfaceIDApp6
107			0	MediaInterfaceIDApp6
108			0	LaneCountApp6
109			0	HostLaneAssignmentOptionsApp6
110			0	HostInterfaceIDApp7
111			0	MediaInterfaceIDApp7
112			0	LaneCountApp7
113			0	HostLaneAssignmentOptionsApp7
114			0	HostInterfaceIDApp8
115			0	MediaInterfaceIDApp8
116			0	LaneCountApp8
117			0	HostLaneAssignmentOptionsApp8

Figure 2, Application Advertising

As shown in the table above, the SLT0OPS4400GT85C supports 5 applications:

400GBASE-SR4, 200GBASE-SR4, 100GBASE-SR4, 2X200GBASE-SR2, 4X100GBASE-SR1

Application Selection and Instantiation

The host can select Applications by programming the AppSel value in Staged Set 0. AppSel=1 is the default Application populated in the Active Control Set at power-on or reset.

**Note that the channels of the module are independent and can be configured separately. (ie. up to four 100GBASE-SR instances can be configured), however, it does not support different applications with different channels at the same time*

FHMD-85SRC supports two methods of application selection and instantiation. The first method is implemented according to CMIS, and the second method is customized, which is simpler.

◆ First method:

The applications switching configuration sequence is as follows: read Application Descriptor Registers and select the required Appsel. Write application configuration to DPConfigLane<i> in Stage Control Set 0, then write 1 to ApplyDPInitLane<i> to trigger Application Instantiation.

The Active Set can be read from page11h. For example,

select AppDescriptor3:

Step 1: Write 0x30 in Page10h Byte145~Byte152(8 bytes)—Set AppselCode3

Step 2: Write 0xFF in Page10h Byte143—Set trigger register to run Application Instantiation.

◆ Second method:

Set the value of Page10h Byte240. This is a private definition.

Code Value	Bit Pattern	Host Electrical Interface	Media Interface
0	00000000b	100GAUI-1-S C2M	100GBASE-SR1
1	00000001b	200GAUI-4	200GBASE-SR4
2	00000010b	100GAUI-4	100GBASE-SR4
3	00000011b	400GAUI-4-S C2M	400GBASE-SR4
4	00000100b	200GAUI-2-S C2M	200GBASE-SR2

Figure 3, Private Host Electrical Interface Codes

TX & RX Squelch

Default TX and RX auto-squelch is enabled. But TX and RX auto squelch disable, and force squelching function are not supported.

TX input equalization

Default TX adaptive equalization is enabled. But TX adaptive equalization disable, and fixed equalization adjust function are not supported.

RX output Equalization

RX output Equalization follows CMIS Table 6-7, with default 1dB, readable and writable

Rx Output Equalization Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	Reserved	Reserved
11-15	1011b-1111b	Custom	Custom

Figure 4, Rx Output Equalization code table

RX output amplitude

RX output amplitude follows CMIS Table 6-8, Rx output amplitude is the difference peak-to- peak EYE high when Rx output equalization is set to 0dB. The default value of output amplitude is set to 2, with typical differential 600mVp-p.

Table 6-8 Rx Output Amplitude Codes

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)
4-14	0100b-1110b	Reserved
15	1111b	Custom

Figure 5, Rx Output Amplitude code table

Loopback capabilities

Media side input loopback and Host side input loopback feature are supported, loopback control method refers to CMIS.

Byte	Bits	Field Name	Field Description
13h:128	6	Simultaneous Host And Media Side loopbacks	0b: not supported
	5	Per Lane Media Side Loopbacks	1b: supported
	4	Per Lane Host Side Loopbacks	1b: supported
	3	Host Side Input Loopback	1b: supported
	2	Host Side Output Loopback	1b: supported
	1	Media Side Input Loopback	1b: supported
	0	Media Side Output Loopback	1b: supported

Figure 6, Rx Output Equalization code table

IX. Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

Parameter	Accuracy	Unit
Internally measured transceiver temperature ¹	+/-3	。 C
Internally measured transceiver supply voltage	+/-3	%
Measured Tx bias current	+/-10	%
Measured Tx output power ²	+/-3	dB
Measured Rx received average optical power	+/-3	dB

Figure 7, Digital Diagnostic Monitor Accuracy

Notes:

1. Test point is the hotspot of the module.
2. DDM reports stability within 0.5 dB when temperature is stable. TX DDM reports -40 dBm when TX disable.

X. Pin Assignment and Description

QSFP112 Transceiver Pad Layout, and PIN Descriptions are as follows:

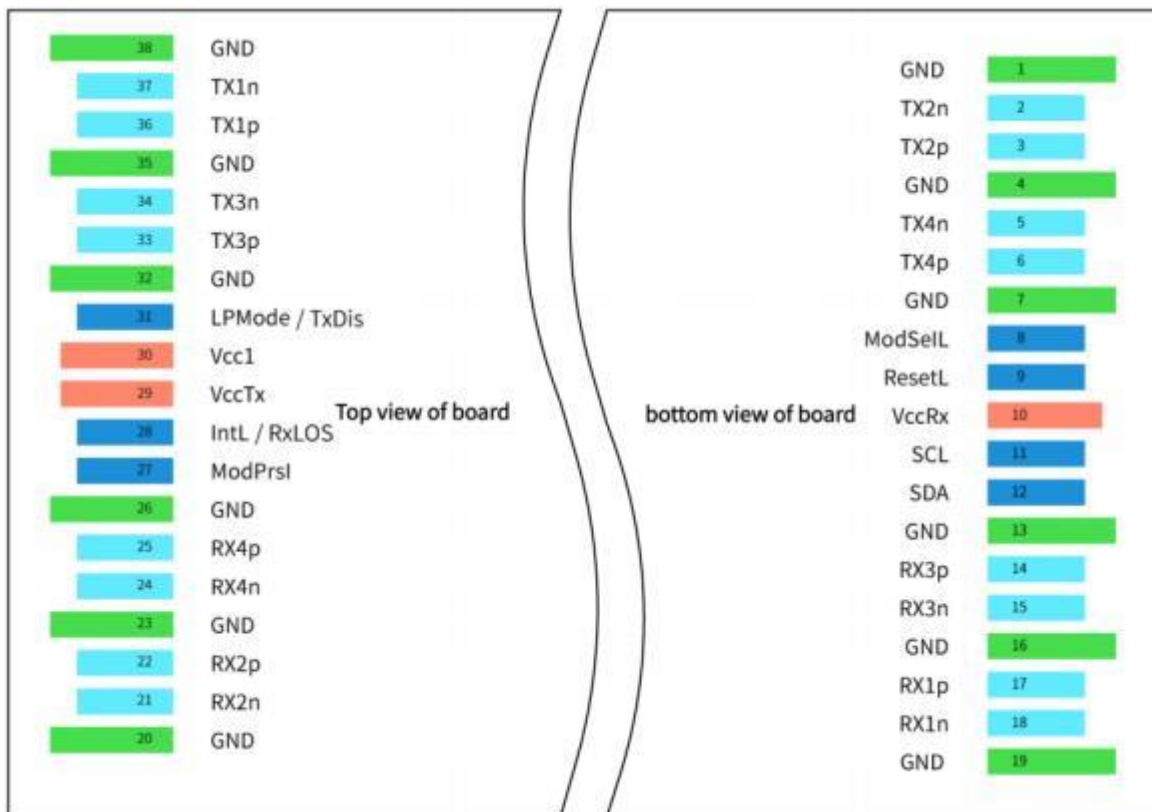


Figure 8, QSFP112 Transceiver Electrical Pad Layout

Pin	Name	Logic	Description	Power Sequence	Notes
1	Ground		GND	1B	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	3B	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	3B	
4	Ground		GND	1B	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	3B	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	3B	
7	Ground		GND	1B	1
8	ModSelL	LVTTL-I	Module Select	3B	
9	ResetL	LVTTL-I	Module Reset	3B	
10	VccRx		+3.3V Power Supply Receiver	2B	2
11	SCL	LVC MOS-I/O	2-wire serial interface clock	3B	
12	SDA	LVC MOS-I/O	2-wire serial interface data	3B	
13	Ground		GND	1B	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	3B	
15	Rx3n	CML-O	Receiver Inverted Data Output	3B	
16	Ground		GND	1B	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	3B	
18	Rx1n	CML-O	Receiver Inverted Data Output	3B	
19	Ground		GND	1B	1
20	Ground		GND	1B	1
21	Rx2n	CML-O	Receiver Inverted Data Output	3B	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	3B	
23	Ground		GND	1B	1
24	Rx4n	CML-O	Receiver Inverted Data Output	3B	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	3B	
26	Ground		GND	1B	1
27	ModPrsL	LVTTL-O	Module Present	3B	
28	IntL	LVTTL-O	Interrupt	3B	
29	VccTx		+3.3V Power supply transmitter	2B	2
30	Vcc1		+3.3V Power supply	2B	2
31	LPMODE	LVTTL-I	Low Power mode	3B	
32	Ground		GND	1B	1

33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	3B	
34	Tx3n	CML-I	Transmitter Inverted Data Input	3B	
35	Ground		GND	1B	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	3B	
37	Tx1n	CML-I	Transmitter Inverted Data Input	3B	
38	Ground		GND	1B	1

Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and VccTx are the receiver and transmitter power supplies and shall be applied concurrently. VccRx, Vcc1 and VccTx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).

XI. Mechanical

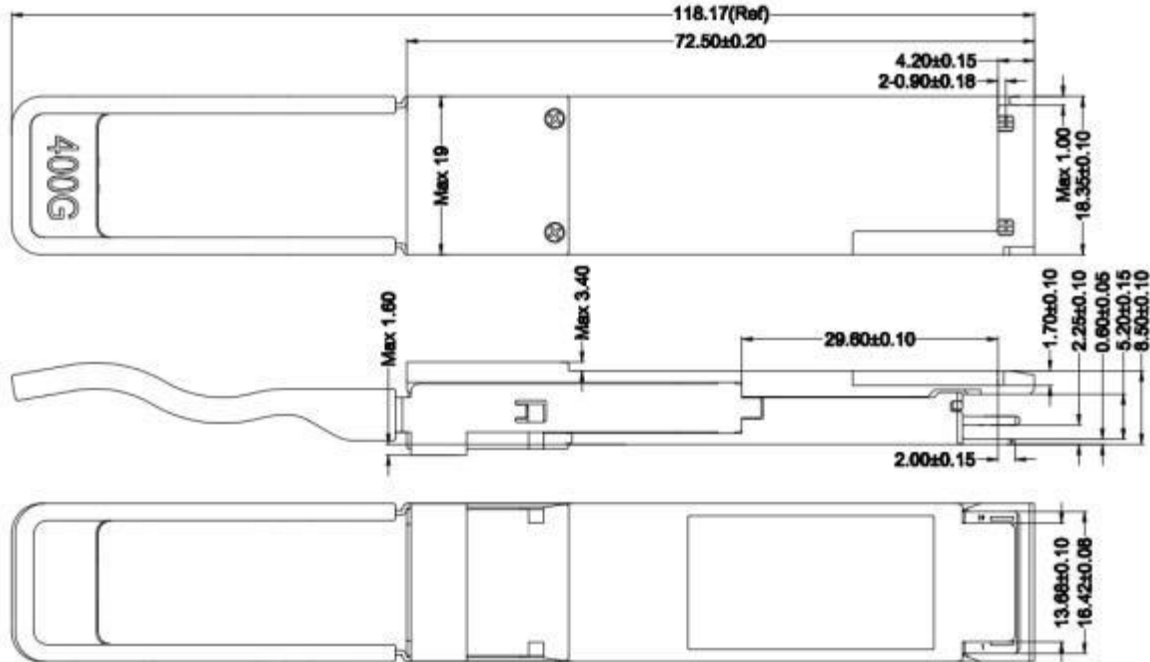


Figure 9, Mechanical Diagram

Optical interface requirement

The optical port provide MPO12 APC as follow:

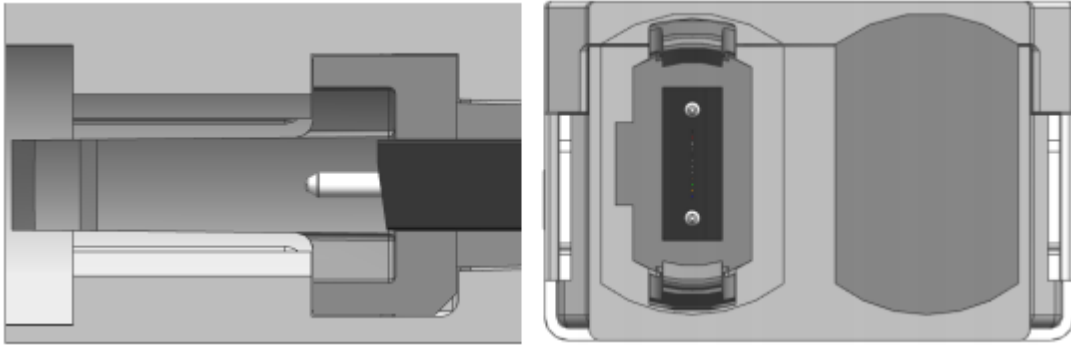


Figure 10, MPO12 APC connector fiber lane assignments

XII. Revision history

Version	Initiated	Reviewed	Revision	Release Date
A0	Tony	Jack	New Release	2023-09-09

XIII. Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD).

A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

XIV. Contact Information

Sales@suliton.com